Storing Usable, Excess Power from TSV Integrated Circuits

The layout of integrated circuits is usually two dimensional in nature, which has hindered progress in scaling circuits to a smaller size. One present solution has been to “stack” the integrated circuits into multiple layers in the same semiconductor die - Three Dimensional (3D) integrated circuits. One method of stacking integrated circuits is through silicon vias (TSV) wherein a 3D-IC is built by stacking silicon wafers and/or dies and interconnecting them vertically so that they behave as a single device. In current TSV systems, when a TSV is placed in a chip for signal or power, it is necessary to surround the TSV with other TSVs that act as a shield to block the signal from interfering with other circuitry. The energy transferred from one TSV to another is typically shunted to ground and the power is lost. However, researchers at the University of Louisiana at Lafayette (UL Lafayette) have developed a strategy to scavenge power from the signal TSVs, which would otherwise be shunted to ground, and store this power for utilization with the integrated circuit.

UL Lafayette understands the value of this research and technology to 3D-IC chip design. Moreover, we understand that for successful commercial implementation, significant industry acumen & perspective will be needed. Accordingly, we currently seek a commercial partner interested in licensing and/or sponsored-research opportunities. To learn more about this technology, please contact Dr. Seth Boudreaux, Associate Director of the Office of Innovation Management via the info provided below.

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